56232-109-CPCK-042

APPLICATION

FOR

UNITED STATES LETTERS PATENT

SPECIFICATION

TO ALL WHOM IT MAY CONCERN:

Be it known that MICHAEL AMATO, a U.S. citizen, residing in Newburyport, Massachusetts, has invented certain improvements in a **HIGH VOLTAGE SEMICONDUCTOR DEVICE HAVING AN INCREASED BREAKDOWN VOLTAGE RELATIVE TO ITS ON-RESISTANCE** of which the following description in connection with the accompanying drawings is a specification, like reference characters on the drawings indicating like parts in the several figures.

HIGH VOLTAGE SEMICONDUCTOR DEVICE HAVING AN INCREASED BREAKDOWN VOLTAGE RELATIVE TO ITS ON-RESISTANCE

Field of the Invention

[0001] The present invention relates generally to semiconductor devices and, more particularly, to a semiconductor device having an increased breakdown voltage relative to its on-resistance.

Background of the Invention

[0002] Planar, vertical, high-voltage, power MOSFETs are typically constructed using N- on N+ epitaxial substrates. Such a device 10 is shown in Fig. 1. Device 10 includes an N- substrate 12 on which an N+ epitaxial layer is grown. The source and gate components 16 of the device 10 are then constructed on the expitaxial layer 14. In such devices, it is desirable to reduce the on-resistance of the device while maintaining the breakdown voltage at a reasonable level. The on-resistance of the device is a function of the voltage rating of the material that forms the epitaxial layer, such that a higher voltage rating results in a higher on-resistance for the device, as shown in Fig. 2. Since the voltage rating is a function of the doping density and the thickness of the epitaxial layer, for a given doping density, the thickness of the epitaxial layer can be manipulated to vary the on-resistance of the device.

[0003] In lower voltage power transistors, such as shown at 20 in Fig. 3 and 21 in Fig. 4, the epitaxial layers 22 and 23, respectively, are relatively thin. In device 20, Fig. 3, the gate 24 is recessed into the epitaxial layer 22 as shown. A trench 26 is formed in the substrate 28, which serves to lower the device on-resistance by reducing the JFET pinch effects. However, because the epitaxially layer 22 under the gate 24 is similar in thickness to the epitaxial layer 14 in device 10, Fig. 1, the improvement in on resistance is marginal. In device 21, Fig. 4, the epitaxial layer 23 is trenched and the gate 25 is recessed to reduce the JFET pinch resistance and improve the channel packing density. In devices 20 and 21, the breakdown voltage of the device may be lowered by the increased exposure of the gate to the epitaxial region defined by each of the thicknesses T_{B2} and T_{B3}.

[0004] In some high-voltage devices, such as is shown at 40 in Fig. 5, in order to increase the breakdown voltage of the device, the epitaxial layer 42 is formed to be relatively thick and is of a relatively lower doping density. A trench 44 may be included in the substrate 46. However, the epitaxial region is planarized during the epitaxy growth period, and this configuration causes the on-resistance of the device to be higher than the planar device 10 of Fig. 1 for an equivalent doping density and thickness T_{B1} and T_{B4}, since T_{A4} is now larger than T_{A1}.

[0005] These and other attempts at improving the on resistance of the power transistor do so by improving the efficiency of the current flow from the top of the epitaxy layer to the substrate. However, they do not change the relationship between the thickness and doping of the epitaxial layer and the maximum breakdown of the device structure.

Summary of the Invention

[0006] The present invention is directed to a semiconductor configuration which enables the devices formed thereon to have increased breakdown voltages without increasing the on-resistance of the devices, or to reduce the on resistance of the device while the breakdown voltage is maintained. In the active region of the semiconductor device, the substrate is formed to be thicker than in the termination region of the device. This results in the epitaxial layer being thinner in the active region than in the termination region. This configuration results in the breakdown voltages of the devices being increased without increasing the on-resistance of the devices.

[0007] This configuration also allows the epitaxial layer to be thinner in the active region while maintaining the doping density without reducing the breakdown voltage. These two methods of breakdown and/or on resistance improvement are compatible with other techniques for reducing on resistance, such as, but not limited to, devices described in the prior art.

[0008] Furthermore, the die surface area required to terminate the high voltage device is significantly reduced. This is because the termination efficiency of the new device can be less than that of the prior art device, since the parallel plane breakdown voltage for the termination region can be made many times higher than the parallel plane

breakdown voltage of the active region. To put it more succinctly, the breakdown voltage is equal to the parallel plane breakdown voltage times the termination efficiency, and the higher the efficiency the more device area the termination will consume. A device made in accordance with the present invention increases the parallel plane breakdown voltage of the termination region through an increase in the epitaxial thickness. The efficiency of the termination region can be reduced, thus reducing termination area, as long as the product of the efficiency and parallel plane voltage is higher than the parallel plane voltage of the active region.

[0009] According to one embodiment, a semiconductor device includes a substrate layer having a first dopant density, an epitaxial layer comprising a second dopant density formed on the substrate layer and a semiconductor switch formed on the epitaxial layer, wherein the semiconductor switch comprises an active region of the semiconductor device. A first thickness of the epitaxial layer in the active region is less than a second thickness of the epitaxial layer in a termination region formed peripherally to the active region.

[00010] The semiconductor switch may include a gate electrode formed on an upper surface of the epitaxial layer and the first thickness may be a distance between the upper surface of the epitaxial layer proximate the gate electrode and an upper surface of the substrate layer. The second thickness may be a distance between the upper surface of the epitaxial layer in the termination region and the upper surface of the substrate layer.

[00011] According to another embodiment, a method of forming a semiconductor device includes:

A. forming a mask over a substrate layer comprising a first semiconductor material of a first thickness and having a first dopant density, wherein the mask covers a first portion of the substrate layer;

B. removing the first semiconductor material from the portion of the substrate not covered by the mask to reduce a second portion of the substrate layer to a second thickness;

C. growing an epitaxial layer over the first and second portions of the substrate layer, such that the epitaxial layer comprises a substantially planar surface opposite a surface of the epitaxial layer which is in contact with the substrate layer, wherein the

epitaxial layer includes a first epitaxial portion proximate the first portion of the substrate layer having a first epitaxial thickness and a second epitaxial portion, proximate the second portion of the substrate layer having a second epitaxial thickness; and

D. forming a semiconductor switch on the substantially planar surface of the epitaxial layer proximate the second epitaxial portion;

wherein the first epitaxial thickness is substantially less than the second epitaxial thickness.

[00012] Finally, in accordance with another aspect of the invention, a method of making a semiconductor switching device comprises a substrate layer and an epitaxial layer having at least a portion lying in the active and termination regions of the device and having a desired breakdown voltage and on-resistance. The method comprises:

forming the epitaxial layer such that the epitaxial layer in the active region of the device is significantly thinner than the epitaxial layer in the termination region so as increase its breakdown voltage relative to its on-resistance.

Brief Description of the Drawings

[00013] The foregoing and other objects of this invention, the various features thereof, as well as the invention itself may be more fully understood from the following description when read together with the accompanying drawings in which:

[00014] Fig. 1 is a schematic diagram of a conventional high voltage semiconductor device of the prior art;

[00015] Fig. 2 is a graph showing the relationship between the on-resistance and the voltage rating of a semiconductor device;

[00016] Figs. 3-5 are schematic diagrams of modified low voltage semiconductor devices of the prior art;

[00017] Fig. 6 is a schematic diagram of a conventional semiconductor device of the prior art showing the active and termination regions;

[00018] Fig. 7 is a schematic diagram of a conventional semiconductor device of the prior art showing voltage potential lines present in the termination region during operation of the device;

[00019] Fig. 8 is a schematic diagram of one embodiment of a semiconductor device made according to the present invention;

[00020] Fig. 9 is a flow diagram showing the steps involved in the manufacturing process of the semiconductor device, in accordance with the present invention; and

[00021] Fig. 10 is a graph showing the relationship between the mesa thickness in the epitaxial layer and the breakdown voltage and on-resistance.

Detailed Description

[00022] A typical semiconductor device configuration, shown in Fig. 6, includes many devices 50 formed in an active region 52 of the substrate 54 and a termination region 56 formed peripherally around the active region. During operation of the devices, the equipotential lines in the termination region 56 of the epitaxial layer 54 are curved, as shown at 60, Fig. 7, which reduces the breakdown voltage of the semiconductor devices. Guard rings 62 may be built into the termination 64 of the device, which help to increase the radius of the curved fields, resulting in a greater breakdown voltage. In the active region 66, the equipotential lines are generally planar, and therefore do not have as much of an effect on the breakdown voltage of the device.

[00023] The breakdown voltage of the device, which in one embodiment, may be a VDMOSFET, is generally limited by the 2-D and 3-D effects in the termination region, which are also a function of the epitaxial layer doping and thickness. Typically, because of the curved fields, the breakdown voltage in the termination region is approximately 50-80% of the planar breakdown voltage. The breakdown voltage in the active region of the device is typically the planar breakdown voltage for any given epitaxy doping and thickness. Accordingly, in order to increase the breakdown voltage of the device, the breakdown voltage of the termination region must be increased, without increasing the on-resistance of the device.

[00024] Fig. 8 is a schematic diagram of a semiconductor device 100 in accordance with the present invention. In addition to the gate and source configuration similar to that shown in Fig. 1, device 100 includes substrate 102 and epitaxial layer 104, as well as P-type guard rings 106 formed in the epitaxial layer 104. As is shown in Fig. 8, the N+ substrate layer 102 is formed to be thicker in the active region 110 of the device

than it is in the termination region 112. The elevated region 114 of the substrate in the active region 110 causes the thickness T_{A2} between the elevated region 114 and the gate 116 to be significantly less than the thickness T_{C2} between the non-elevated region 118 and the upper surface 120 of the device 100. As an example, a 350V VDMOSFET of device 10 may have an epitaxial layer 104 thickness T_{A1} equal to 35 microns. Reducing T_{A5} of device 100 to 23 microns while maintaining T_{C5} at 35 microns reduces the on resistance of the VDMOSFET 30% while maintaining the breakdown voltage. At this point the active region breakdown and the termination breakdown are equivalent. The relationship between the thickness of the epitaxial layer 104 and the breakdown voltage and on-resistance is shown in Fig. 10. In Fig. 10, the thickness of the substrate 102 or "mesa" (equivalent to T_{C5} minus T_{A5}) in the active region is plotted against the corresponding breakdown voltage for the device. As shown in the figure, an increase in the thickness of the mesa, which results in a decrease in the thickness (T_{A5}) of the epitaxial layer, results in a decrease in the breakdown voltage in the active region and a corresponding decrease in the on-resistance.

[00025] In the preferred embodiment, thicknesses T_{A5} and T_{B5} of device 100 are less than corresponding thicknesses T_{A1} and T_{B1} of device 10 of Fig. 1.

[00026] The difference in the thicknesses T_{A5} and T_{C5} is adjusted so that the breakdown voltage of the device is no longer limited by the edge of the device. In other words, as described above, the breakdown voltage can be maintained while reducing the on resistance by maintaining T_{C5} of device 100 equal to T_{A1} of device 10, but reducing the thickness of T_{A5} of device 100. Conversely, since the voltage rating of the material is a function of the doping density and the thickness of the epitaxial layer, increasing the thickness in the termination region results in a higher breakdown voltage for the device without increasing the on-resistance of the device.

[00027] A method of constructing the device 100 is shown in flow diagram 150 of Fig. 9. First, in step 152, the substrate 102 is masked where the active region is to be formed. The silicon is then removed from the portion of the substrate that is not masked, step 154. This step may be carried out using any known process, such as wet silicon etching or dry etching. Since the angle of the transition between the elevated region 114 and the non-elevated region 118 and the actual location of the transition is not critical to

the operation of the device, the removal of the silicon material outside of the mask can be performed by any known removal method and does not require precise alignment of the mask. The epitaxial layer 104 is then grown on the substrate 102, step 156, and, if necessary, the epitaxial layer is planarized, step 158. When the epitaxial layer is relatively thin, the planarization step may be necessary to provide sufficient offset between the epitaxial layer thickness in the active region and the termination region. Thick epitaxial layers tend to self-planarize during epitaxial growth. Once the epitaxial layer is formed, a conventional device, such as a VDMOSFET, is built on the surface of the epitaxial layer 104 in the active region, step 160.

[00028] Alternatively, the device may be formed through diffusion of dopants into the substrate from the backside of the wafer or from a buried layer in order to build up the substrate 102 in the active region.

[00029] While the invention is described as pertaining to the construction and operation of a VDMOSFET, it will be understood that the invention could also be applied to other semiconductor devices, such as IGBT, Bipolar, diodes and other semiconductor high voltage devices. The invention could also be applied to P- on P+ substrates and other semiconductor materials, such as GaAs and SiC.

[00030] Accordingly, the present invention provides a semiconductor structure that provides devices formed thereon with higher breakdown voltages without increasing the on-resistance of the devices. This is accomplished by forming the substrate and epitaxial layers such that the epitaxial layer in the active region of the device is significantly thinner than the epitaxial layer in the termination region. Alternatively, the on resistance can be lowered while maintaining the desired breakdown voltage.

[00031] The invention may be embodied in other specific forms without departing from the spirit or essential characteristics thereof. The present embodiments are therefore to be considered in respects as illustrative and not restrictive, the scope of the invention being indicated by the appended claims rather than by the foregoing description, and all changes which come within the meaning and range of the equivalency of the claims are therefore intended to be embraced therein.